

DESIGN OF THE PHYSICAL LAYER OF PCI EXPRESS- A REVIEW

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Abstract—PCI Express implements dual simplex link to transmit and receive data simultaneously on transmitter and receiver device. PCI Express employs packet to accomplish data transfer between devices. This paper presents the physical layer architecture of PCI Express 1.0a which ensures reliable transport of transaction layer packets (TLPs) and data link layer packets (DLLPs) on both transmitter and receiver side. The physical layer helps in reliable conveying with start and end bit to each data coming from transaction layer and data link layer on transmitter side and the packet is decoded on receiver side. For simulation of each sub block of both transmitter and receiver we are using Xilinx ISE software & for coding we employed Very High Speed Integrated Circuit Hardware Description Language (VHDL).

Keywords— PCI Express, Physical layer, VHDL.

I. INTRODUCTION

In today's modern era of communication, use of high speed data transfer system is must. Data transfer rate is mainly dependent on the data transfer protocol and the method of communication. These days, all high speed data communication are digital. Digital data communication method is more secure and less interfered by noise. The important thing is to select the protocol used for communication. There are many protocols like SPI, I2C, PCI, PCIE, and USB. PCI Express (Peripheral Component Interconnect Express), is a computer expansion card standard designed to replace the older PCI, PCI -X, and AGP standards [1][2].

PCI-E is the latest standard used in personal computers which was introduced by INTEL. The difference between PCI-E and PCI is that, PCI-E is used for serial data transmission whereas PCI leads to parallel data transmission. PCI Express serve as a general purpose I/O interconnect for a wide variety of future computing and communication platforms. PCI Express is based on serial point-to-point interconnect which reduces the cost and design complexity. The intent of this serial interconnect is to establish very high bandwidth communication [3].

1.1 PCI Express Link

The connection between two PCI-E devices is called as link. Each link is composed of one or more lanes. Each lane

compose of one pair of signals: send and receive. This full-duplex communication is possible because each lane consist of one pair of signals: send and receive. PCI-E supports x1, x4, x8, x12, x16, and x32 link widths. A single lane is capable of transmitting 2.5Gbps in each direction simultaneously.

1.2 Packet Flow

PCI Express uses packet to communicate information between two devices. Packets are formed in the transaction and data link layers to carry the information from transmitter to receiver device. As the transmitted packets flow through the layers, they are extended with additional information necessary to handle packets at those layers. At the receiver side the reverse process occurs and the additional bits are terminated.

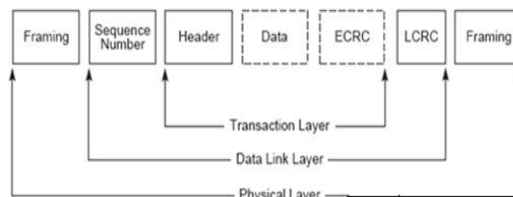


Fig.1. Packet Flow through Layers

1.3 PCI Express Layering Overview

PCI Express is a layered protocol, consisting of a transaction layer, a data link layer, and a physical layer. Each of these layer is divided into two sections: one is the transmitter that processes outbound information and other is the receiver that processes inbound information [7][8].

The Transaction Layer is the topmost PCI Express architecture layer. Its primary function is the assembly and disassembly of transaction layer packets (TLPs), and is responsible for managing credit based flow control of TLPs.

The Data link Layer is the intermediate stage between transaction and data link layer. It provides reliable mechanism for the exchange of TLPs between two components on a link. It also provides service for error detection and recovery [9].

The Physical Layer is responsible for exchanging information with the data link layer in an implementation specific format. It includes drivers and buffers, parallel-to-serial and serial-to-parallel conversion, scrambler circuitry.

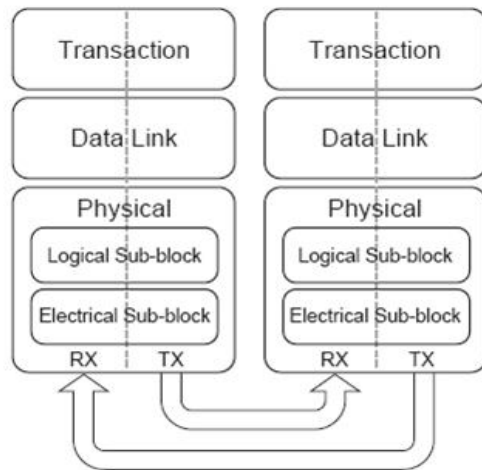


Fig 2 : PCI Express Layering

II. LITERATURE REVIEW

Wang Lihua worked on design of PCI Express Transaction Layer. The author gave the transmitter and receiver flowchart and state transition diagram of Transaction Layer. The implementation was done using Verilog HDL code and test bench for verification and function simulation. The design meets the specification of PCI Express Base specification Revision 2.0. The design determines its correctness and supports the function of PCI Express Transaction Layer [4].

SatishK.Dhawan worked on PCI Express-A New High Speed Serial Data Bus. It is a very high speed dual-simplex, point to point serial differential low voltage interconnect. The signaling rate is 2.5 Gbit per second, with 8/10 bit encoding to embed the clock in the data stream. On the transmit side parallel data is shifted out serially and on the receive side serial data is shifted into registers for parallel data output. The data is shifted serially at 2.5GHZ to the printed circuit board traces or to the cable segment [5].

M. Aguilar, A. Veloz, M. Guzman worked on the Data link Layer of PCI Express. The Data Link Layer of PCI-Express, as is defined in PCI-Express Base Specification Revision 1.0a was design and implemented. The architecture presented here contains the transmission and receiver modules which ensure the reliably conveying of the Transaction Layer Packets (TLP) between two components using the PCI-Express protocol with

the addition of sequence number and a 32-bit CRC to each TLP in transmit side and its reverse operation in receiver side [6].

III. DESIGN METHODOLOGY

Understanding of PCI Express 1.0a Physical Layer architecture .According to the specification mentioned, designing each sub-blocks of Physical layer using VHDL. The test bench verification is done to verify the correctness of the design module and its function simulation.

3.1 Physical Layer Design

The proposed physical layer architecture consists of both transmitter and receiver.

3.1. a. Transmitter

Transmit buffer receives TLPs and DLLPs from data link layer. The physical layer frames the packet with start and end character using control signal.

With the aid of multiplexer, the packet data is framed with start and end character. The receiver device used to detect framing symbols (start and end of packet).

The scrambler uses an algorithm to pseudo randomly scramble each byte of packet. The start and end framing bytes are not scrambled. It eliminates repetitive patterns in the bit streams, which leads to EMI noise generation. Scrambling spreads energy over a frequency range and minimise noise.

The 8b/10b Encoder encodes the scrambled 8 bit character into 10 bit symbols. These are then converted into serial bit stream by the parallel-to-serial converter.

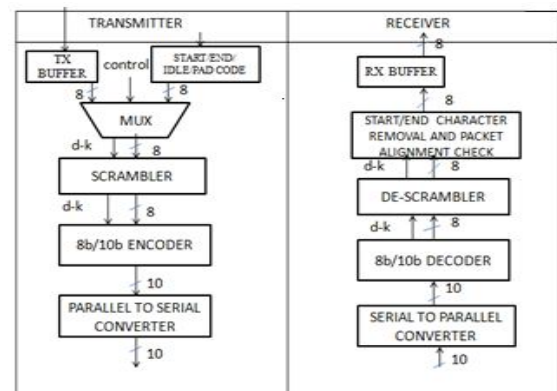


Fig 3 : Shows the Physical Layer diagram

3.1. b. Receiver

The high speed deserializer on the receiver side converts the received serial data stream from serial-to-parallel.

The 10b symbol is converted back to 8b character by the 8b/10b decoder. It eliminates the start and end characters, that frames the packet and also look for errors.

The De-scrambler reproduces the de-scrambled packet stream from the incoming scrambled packet stream. It implements the inverse of the algorithm implemented in the transmitter scrambler.

The byte stream is then loaded into receiver buffer to feed to the data link layer.

IV. CONCLUSION AND FUTURE WORK

This paper presents the design of PCI Express Physical layer architecture. The paper determines various sub-block functions of physical layer. It also depicts about peer-to-peer communication for transmitting data in serial manner between transmitter and receiver device. The PCI Express can become more compatible and scalable with less noise interference due to serial technology. An improvement in PCI Express transfer rate can greatly improve system performance.

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